

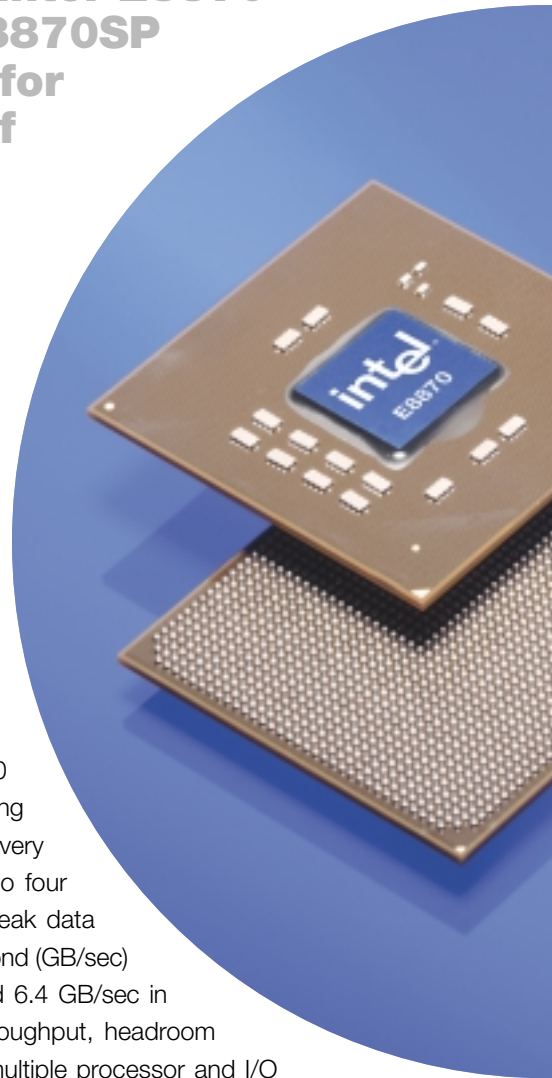


Can a scalable, building block architecture provide the heavy lifting required for the demanding applications of today?

Yes. The highly scalable Intel® E8870 chipset, featuring the E8870SP component, is designed for the heavy lifting needs of applications today, and gives your platform room to grow to meet the challenges of tomorrow.

Platform Overview

The Intel® E8870 chipset building blocks, featuring the E8870SP component, build upon its single node platform predecessor and allows for multi-node configurations of up to eight Intel® Itanium® 2 processors. This added processor and I/O headroom is essential to systems used for large database, business intelligence, Enterprise Resource Planning (ERP) and other high-end, heavy load applications. The highly reliable and serviceable building block architecture of the E8870 chipset provides excellent return on investment allowing the system to grow with your business needs. In every processor node, the system bus can support up to four Itanium 2 processors with 400 Megahertz (MHz) peak data transfer rate, providing up to 6.4 Gigabytes per second (GB/sec) bandwidth. With an 800 MHz channel frequency and 6.4 GB/sec in bandwidth, the memory bus provides excellent throughput, headroom and improved scalability. The E8870SP connects multiple processor and I/O nodes through 6.4 GB/sec scalability ports. This balanced architecture provides processing and I/O headroom, low system latency, high bandwidth transactions and delivers high availability and optimal performance to demanding server workloads.



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Functional Overview of the Intel E8870 Chipset Components

The E8870SP Scalability Port Switch (SPS)

enables scaling of the SNC and SIOH building blocks into a bigger Symmetric Multi-Processing, or SMP, system. It allows the Original Equipment Manufacturer to build up to 2-node, 8-processor systems using two SPS, two SNC and two SIOH components.

The SPS fulfills two key functionalities: providing the necessary interconnect for moving data to and from the constituent building blocks and ensuring memory coherency in the system. The SPS has a built-in crossbar interconnect and bypass busses for critical coherent traffic and a built-in central snoop filter architecture to preserve coherency while minimizing snoops to remote nodes.

The Intel E8870 building block architecture allows the platform architecture to scale well beyond an 8-way system by enabling the use of SP-based proprietary switch technology. These larger platforms can take advantage of the SNC and SIOH building blocks, allowing the next level of scalability and availability.

The Intel E8870 chipset Scalable Node Controller (SNC) is the central component in the processor/memory sub-system, with interfaces to the processor, the memory subsystem, firmware and two Scalability Ports for access to I/O and remote memory.

The SNC connects to four DDR Memory Hubs via four links providing a peak memory bandwidth of 6.4 GB/sec. The SNC can buffer up to 8 Kilobytes (KB) of write data to prioritize reads over writes, and implements interleaving and re-ordering to improve bandwidth and reduce latency. Each DDR Memory Hub connects to two branch channels and supports up to four DDR SDRAM DIMMs per channel. Up to 128GB of memory per SNC is supported using thirty-two 4GB DIMMs.

The Scalability Port, or SP, provides simultaneous, bi-directional signaling with 3.2 GB/sec peak bandwidth per direction or an aggregate bandwidth of 6.4 GB/sec per port. Two SP ports per SNC provide a maximum bandwidth capability of 12.8 GB/sec. Together, these advanced features of the SNC deliver balanced, high-bandwidth throughput across the processors, memory and I/O.

The E8870DH DDR Memory Hub (DMH) bridges data transfers between the SNC and two DDR memory channels. Each DMH delivers a maximum throughput of 1.6 GB/sec supporting up to eight single or double density registered DIMMs. This provides up to 32 GB of DDR memory per DMH when configured with 1 Gigabit memory devices.

The E8870IO Server Input/Output Hub (SIOH)

is the central component of the I/O subsystem for Intel E8870 chipset-based servers. This component provides the connection between four Hub Interface 2.0 ports and two Scalability Ports. Each Hub Interface has a peak bandwidth of 1 GB/sec. The aggregate peak bandwidth of the SIOH with four Hub Interfaces is 4 GB/sec. The SIOH has internal mechanisms to optimize data throughput on all interfaces and has a pre-fetch engine and internal read cache to deliver full bandwidth on data return. The SIOH also offers a Hub Interface 1.5 connection to legacy I/O and firmware via the I/O Controller Hub (ICH4).

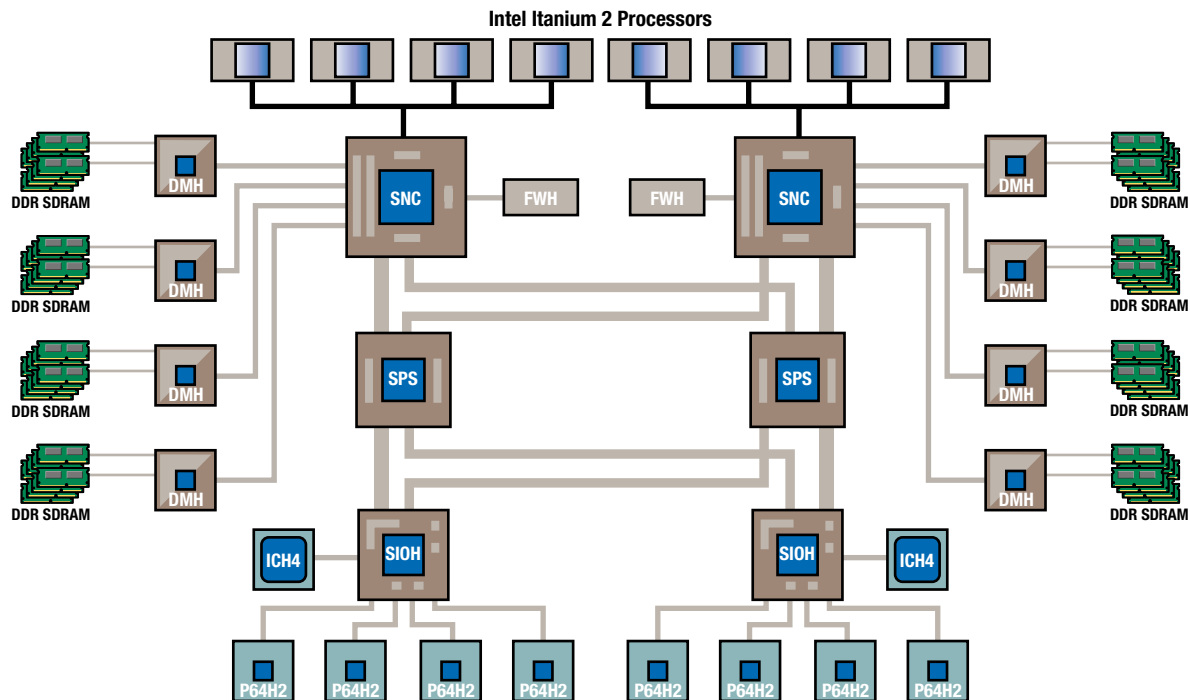
The Intel® 82870P2 64-bit PCI/PCI-X Controller Hub 2 (P64H2) introduces the high-performance PCI-X bus to the enterprise server market. This second-generation component provides bridging functions between the SIOH and the latest PCI-X peripherals. The P64H2 connects to the SIOH through one of the four Hub Interface 2.0 ports, delivering a maximum throughput of 1 GB/sec on each connection. Each P64H2 contains two independent high-performance 64-bit PCI/PCI-X interfaces capable of up to 133 MHz operation. The P64H2 also integrates two hot plug controllers, one for each interface. A fully populated platform configuration using four P64H2 components can support up to eight 64-bit, 133 MHz PCI-X devices.

The P64H2 allows I/O configuration flexibility through the addition of the Intel® 82544GC Gigabit Ethernet controller and the Intel® I/O processor. The Intel® Gigabit Ethernet controller provides the high network throughput of Intel's Gigabit Ethernet products in a single, integrated component. The Ethernet controller incorporates a 133 MHz, 64-bit wide PCI-X interface that matches the I/O bandwidth of the P64H2 component. The small size and low power consumption of this Ethernet controller make it ideal for LAN on motherboard platform implementations.

The Intel® 82801DB I/O Controller Hub (ICH4)

connects to the SIOH through the Hub Interface 1.5 port. The ICH4 contains the legacy I/O interfaces required by a system. Flash memory, keyboard, USB, and IDE are typical I/O devices attached to the ICH4. The ICH4 offers a 2-channel Ultra ATA/100 bus master IDE controller, a USB 2.0 controller supporting up to six USB ports, a 32-bit PCI 2.2 compliant interface and a SM bus controller for system manageability.

8-way Itanium® 2-based System



Features that Maximize Performance and Balance the Platform

Feature	Benefit
Balanced Chipset Architecture	<ul style="list-style-type: none"> Delivers optimal system performance through well aligned bandwidths. (System bus, memory, SP & I/O bandwidths are well balanced)
Support For Multiple Intel® Itanium® Processor Family Generations	<ul style="list-style-type: none"> Platform longevity
Data ECC Protection Across Key Interfaces	<ul style="list-style-type: none"> Provides enterprise-class data integrity across multiple nodes
Built-in Central Snoop Filter Architecture Of The E8870SP	<ul style="list-style-type: none"> Preserves coherency while minimizing snoops to remote nodes
400 MHz, 128 Bit System Bus Capability	<ul style="list-style-type: none"> 6.4 GB/sec system bus supports up to four Intel® Itanium® 2 processors for optimal system performance
High Memory Capacity	<ul style="list-style-type: none"> The DMH provides a maximum of eight DIMM slots with an aggregate of thirty two memory slots enabled per processor node. Maximum capacity supported per processor node is 128GB using 4GB DIMMs
Two High-Bandwidth Scalability Ports Per SNC & SIOH	<ul style="list-style-type: none"> Provides sufficient system headroom for single-node, multiple node and degraded configurations
Hub Interface 2.0 Connectivity	<ul style="list-style-type: none"> Delivers 1 GB/sec bandwidth per connection providing multiple I/O configuration options and offering both flexibility and performance
I/O Prefetch Engine And Built-In Cache	<ul style="list-style-type: none"> Delivers full bandwidth on data return
High Performance PCI/PCI-X Bridge Support	<ul style="list-style-type: none"> Provides support to all PCI/PCI-X I/O devices, from legacy PCI to higher performance PCI-X at 133 MHz
Advanced Platform RASUM	<ul style="list-style-type: none"> ECC protection & correction, memory scrubbing, Memory Device Failure Recovery (MDFR), multiple redundant I/O paths and error logging combine to yield a more reliable platform, reducing downtime for repair and ensuring data integrity across all interconnects and busses

Products

Package

E8870SP	Scalability Port Switch (SPS)	1012-pin 10 Layer Organic LAN Grid Array-2B (OLGA)
E8870	Scalable Node Controller (SNC)	1357-pin Organic LAN Grid Array-2B 12L (OLGA)
E8870DH	DDR Memory Hub (DMH)	567-pin Organic LAN Grid Array-1 6L (OLGA)
E8870IO	Server Input Output Hub (SIOH)	1012-pin 10 Layer Organic LAN Grid Array-2B (OLGA)
82870P2	64-bit PCI/PCI-X Controller (P64H2)	567-pin Flip Chip Ball Grid Array-6L (FCBGA)
82801DB	I/O Controller Hub (ICH4)	421-pin Micro Ball Grid Array (uBGA)
82802AC	FirmWare Hub (FWH)	32-pin Plastic Leaded Chip Carrier (PLCC)

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developer.intel.com/design/itanium2

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